

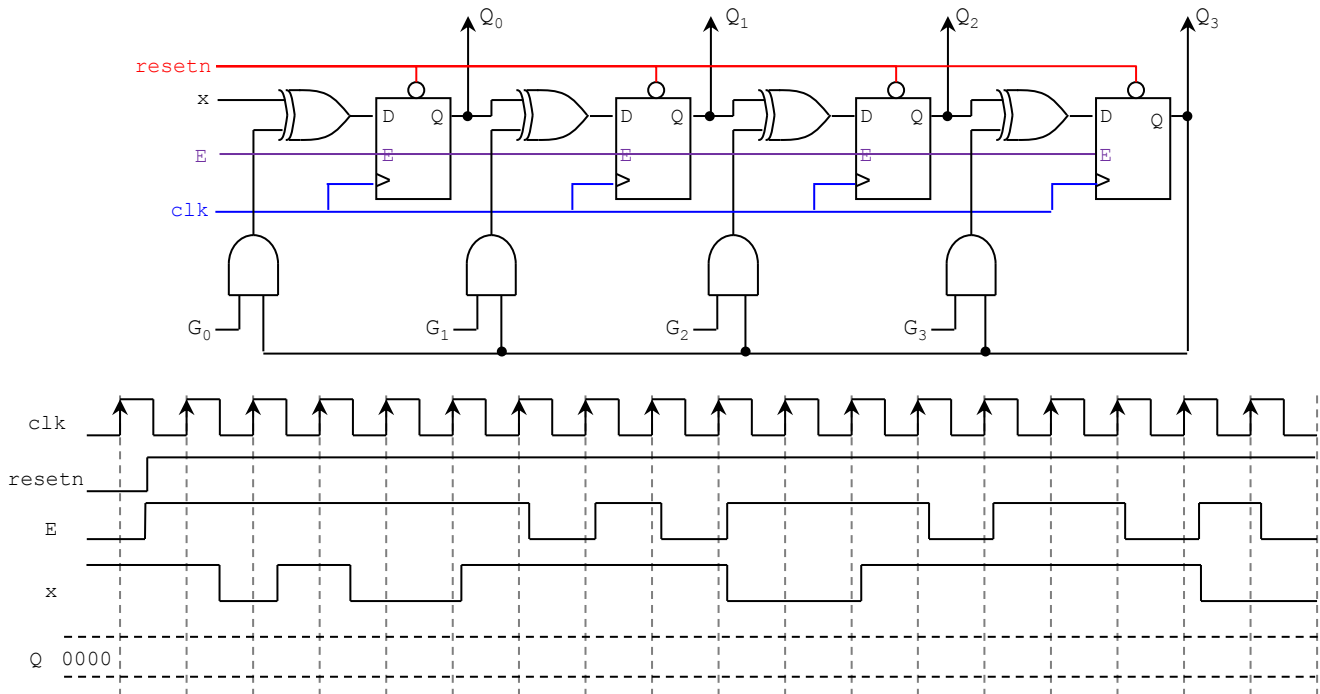
Final Exam

(April 18th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

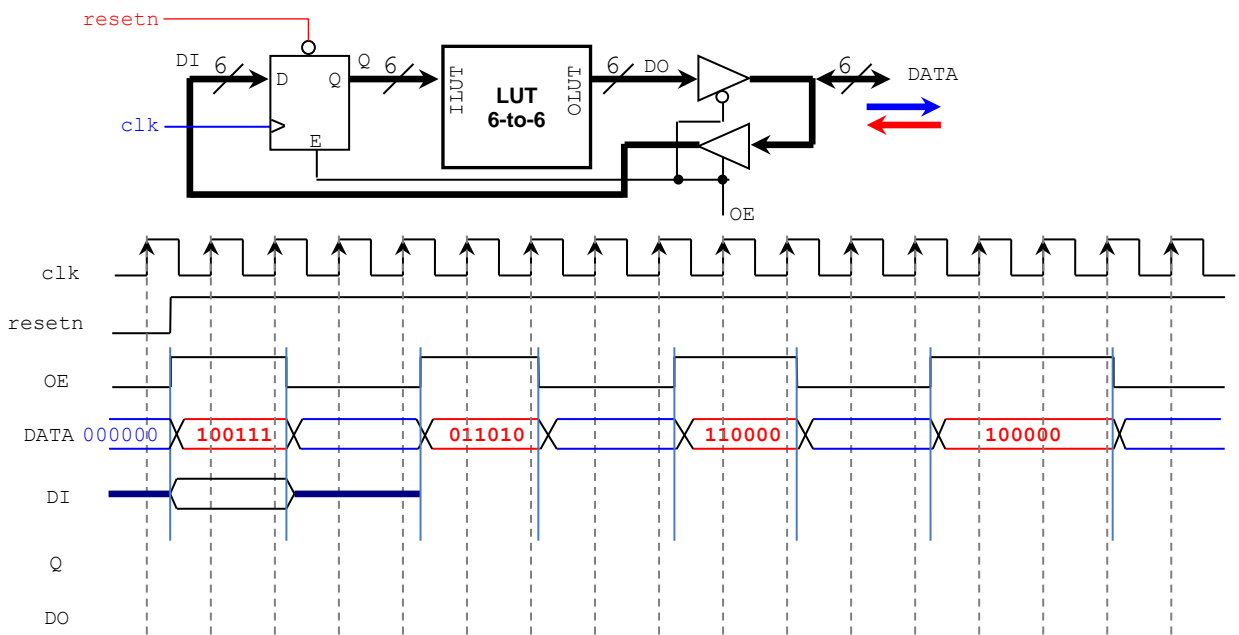
PROBLEM 1 (12 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 0110$, $Q = Q_3Q_2Q_1Q_0$



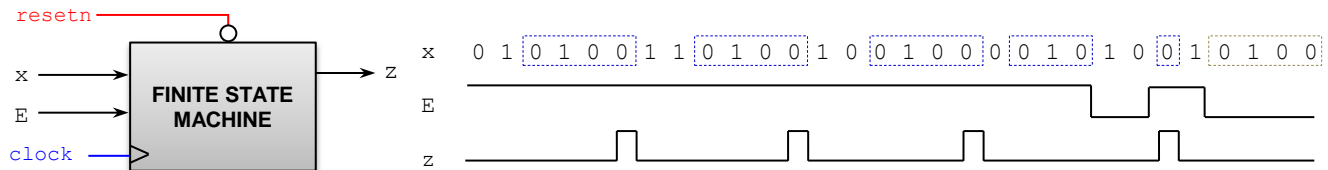
PROBLEM 2 (11 PTS)

- Given the following circuit, complete the timing diagram.
The LUT 6-to-6 implements the following function: $OLUT = |ILUT|$ (absolute value), where $ILUT$ is a 6-bit signed (2C) number, and $OLUT$ is a 6-bit unsigned number.
For example $ILUT = -29 = 10011_2 \rightarrow OLUT = |-29| = 29 (011101_2)$



PROBLEM 3 (24 PTS)

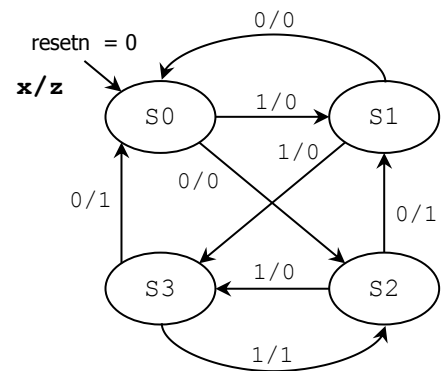
- Sequence detector: The machine generates $z = 1$ when it detects the sequence 0100. Once the sequence is detected, the circuit looks for a new sequence.
- The signal E is an input enable: It validates the input x , i.e., if $E=1$, x is valid, otherwise x is not valid.



- Draw the State Diagram (any representation) of this circuit with inputs E and x and output z . (7 pts)
- Complete the State Table and the Excitation Table (8 pts.)
- Provide the excitation equations and the Boolean output equation (simplify your circuit: K-maps or Quine-McCluskey).
- Sketch the circuit. (3 pts)
- Which type is this FSM? (Mealy) (Moore) Why? _____

PROBLEM 4 (22 PTS)

- a) Given the following State Machine Diagram: (11 pts)
- ✓ Provide the State Table and the Excitation Table (4 pts.)
 - ✓ Get the excitation equations and the Boolean equation for z . (3 pts.)
Use S_0 ($Q=00$), S_1 ($Q=01$), S_2 ($Q=10$), S_3 ($Q=11$) to encode the states.
 - ✓ Sketch the Finite State Machine circuit. (3 pts.)
 - ✓ Which type is this FSM? (Mealy) (Moore)

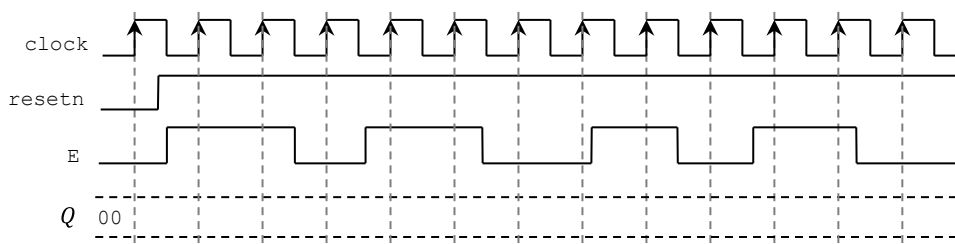


- b) A synchronous circuit (with $resetrn$ and $clock$), is described by these excitation equations (E is a synchronous input): (11 pts.)

$$Q_1(t+1) \leftarrow Q_1(t) \cdot \overline{Q_0(t)} + \overline{E} \cdot Q_1(t) + \overline{Q_1(t)} \cdot Q_0(t)$$

$$Q_0(t+1) \leftarrow E \cdot Q_0(t) + \overline{E} \cdot \overline{Q_0(t)}$$

- ✓ With flip flops and logic gates, sketch the circuit.
- ✓ Complete the timing diagram. $Q = Q_1Q_0$ (Tip: get the excitation table) (6 pts)



PROBLEM 5 (13 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. (7 pts.)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
    port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```

```
architecture behavioral of circ is
    type state is (S1, S2, S3);
    signal y: state;
begin
    Transitions: process (resetn, clk, r, p, q)
    begin
        if resetn = '0' then y <= S1;
        elsif (clk'event and clk = '1') then
            case y is
                when S1 =>
                    if r = '0' then
                        y <= S2;
                    else
                        if p = '1' then y <= S3; else y <= S1; end if;
                    end if;

                when S2 =>
                    if q = '1' then y <= S1; else y <= S3; end if;

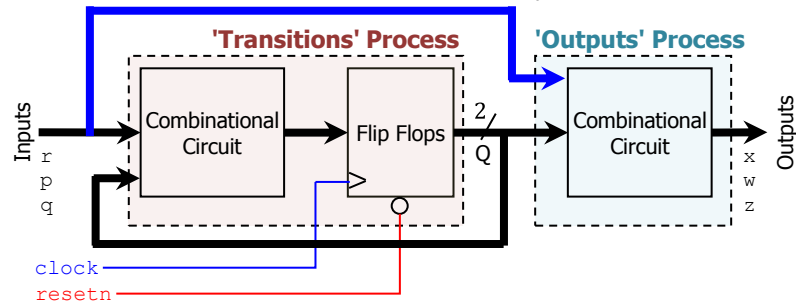
                when S3 =>
                    if p = '1' then y <= S3; else y <= S2; end if;
            end case;
        end if;
    end process;

    Outputs: process (y, r, p, q)
    begin
        x <= '0'; w <= '0'; z <= '0';
        case y is
            when S1 => w <= '1';
                        if r = '1' then x <= '1'; end if;

            when S2 => if p = '1' then x <= '1'; end if;
                        if q = '0' then z <= '1'; end if;

            when S3 => if p = '0' then x <= '1'; end if;
        end case;
    end process;
end behavioral;
```

- The figure shows an FSM model representing the circuit described in VHDL. The state (signal 'y' in the VHDL code) is represented by the bits Q_1 and Q_0 .



- ✓ If we use S1 ($Q=00$), S2 ($Q=01$), S3 ($Q=10$) to encode the states, what is the Boolean equation for w ? (2 pts.)

$w =$

- ✓ Circle the correct answer: (4 pts.)

- | | | |
|---|---------------------|-----------------|
| <ul style="list-style-type: none"> ▫ The 'Outputs' process outputs depend on clock and resetn? | TRUE | FALSE |
| <ul style="list-style-type: none"> ▫ The relationship between $[r, p, q, \text{present state}]$ and $[\text{next state}]$ is described by: | Transitions Process | Outputs Process |
| <ul style="list-style-type: none"> ▫ The relationship between $[r, p, q, \text{present state}]$ and $[\text{outputs } x, w, z]$ is described by: | Transitions Process | Outputs Process |
| <ul style="list-style-type: none"> ▫ Is this a Mealy or a Moore FSM? | Moore | Mealy |

PROBLEM 6 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a Datapath circuit.
- The behavior (on the clock tick) of the generic register is as follows:

4-bit register: If E=0, the output is kept

```

if E = 1 then
  if sclr = 1 then
    Q ← 0
  else
    Q ← D
  end if;
end if;

```

